Gate Oxide Electrical Stability of p-type diamond MOS capacitors

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***Abstract*—This work shows the effect of performing consecutive measurement prior to negative bias stress instability on diamond metal-oxide-semiconductor capacitor (MOSCAP). For the first time, time-dependent stress tests have been carried out in order to investigate the stability of the flatband voltage (V_{FB}) of MOSCAPs through capacitance-voltage (CV) measurements. Two test have been performed. In the first test, consecutive CV measurements with the device biased from deep depletion to the accumulation regime was performed to monitor the recovery of the V_{FB}. In the second test, Negative Bias Stress Instability (NBSI) technique has been applied. V_{FB} stability has been measured by means of a time dependent bias stress in which the device was polarized at a fixed negative voltage for a specific time interval prior performing the next CV measurement. As V_{FB} is directly connected to the effective oxide charge (N_{eff}), the two different tests allowed the extraction of total amount of N_{eff} that interfered during the measurements. The result observed shows that the post-oxidation annealing process induces a strong enhancement of the MOSCAP stability together with a decrease of N_{eff}.**

***Index Terms*— Diamond, Flatband voltage, Oxide reliability, Metal Oxide Semiconductor Interface.**

I. Introduction

Semiconducting diamond is an attractive candidate for the next generation of high voltage and high frequency power devices mainly due to its exceptional properties in terms of wide bandgap, high breakdown field and thermal conductivity. Several diamond-based field-effect-transistors (FETs) have shown good I_{on}/I_{off} ratio [1] and high blocking voltage capability (∼2kV) [2] in a wide range of operating temperatures (up to 400°C) [3]. Recent publications have proven the possibility of generating either inversion [4] or deep depletion regime [5] in oxygen terminated diamond metal-oxide-semiconductor FET (MOSFET), paving the way for a new generation of diamond FETs. The potential of these diamond devices will necessitate the study of other design considerations such as complexity, cost, power density and reliability.

Reliability issues relating to widely investigated GaN and SiC power devices are investigated in literature [6-7]. For devices which need a metal oxide semiconductor interface, an obvious reliability concern is the stability of the gate stack. One of the limiting factors in the application of SiC device is the threshold voltage shifts during long term operation and the stability of SiO_2 gate oxide at elevated temperatures. Leslis[22] has proved that the instability in the threshold voltage arises from the oxide trap activation and oxide charge trapping in the gate stack. Improvement in the device processing such as post oxidation annealing has proven to be of significance in device reliability performance. ~~Theoretical demonstrations have shown that based on the intrinsic properties of diamond, a superior performance to can be obtained in diamond MOSFETs SiC MOSFETs~~.

Diamond has often been named as a superior material to SiC for power device applications [19-20] For efficient diamond MOSFETs, a reliable dielectric with stable electrical properties is critical for the device performance. for commercial applications. Aluminum oxide (Al_2O_3) is the most frequently used as the gate oxide for diamonds FETs studies. It gives the lowest interface states density, allowing depletion, deep depletion and inversion mode in diamond [15,16,4]. SiO_2 though with a higher band gap than Al_2O_3 is limited by its relatively lower dielectric constant and slightly smaller breakdown field (look for the MOSCAP fabricated by Geis long time ago, cite as reference). Capacitance and band alignment measurements has shown that Al_2O_3 deposited by atomic layer deposition at high temperature (> 250°C) is favourable for better band alignment [8] and dielectric properties than other high-k oxides on diamond [Ref Yamazaki]. Consequently, a reduction of the gate leakage current has been observed for devices [9, 18]. Studies on Al_2O_3 diamond MOSCAPs have revealed the presence of near interface and oxide charges that could seriously affect the performance and the stability of the

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MOS system. It has also been demonstrated that post-oxidation annealing causes a redistribution of interface traps and reduces the Fermi level pinning at the oxide/diamond interface [10]. However, no work has been reported on the stability and reliability of MOSCAP devices with respect to voltage and time. In this work, the effect of gate voltage-induced-stress on the stability of the flatband voltage (V_{FB}) has been analyzed. This parameter, which is directly connected to the threshold voltage [9], will give information on the quality of the diamond/semiconductor interface and the evaluation of the MOS-based device reliability.

II. EXPERIMENTAL PROCESS

Using a (100) orientated high-pressure high temperature (HPHT) 1b substrate, stack of 700 nm of heavily doped (p++) and 1 µm of lightly doped (p-) boron layers were grown by Microwave Plasma enhanced Chemical Vapor Deposition (MPCVD) to 5 x 10^{20} cm^{-3} and 2 x 10^{17} cm^{-3} respectively. The doping concentration has been confirmed by cathododoluminescence spectroscopy and CV measurements. Following Inductive Coupled Plasma (ICP) etching technique, the ohmic contact was fabricated. Oxygen termination of the diamond surface (O-Diamond) was carried out by oxygen plasma treatment technique [11] before the atomic layer deposition of Al_20_3 (40 nm) at 380°C. The gate contacts were fabricated using Ti, Pt and Au. Metal insulator metal capacitors (MIMCAP) have been incorporated in the fabrication steps to measure the oxide capacitance. A schematic of the fabricated device is shown in fig.1. The samples were annealed in vacuum (10^{-5} mbar) at 500 °C for 30 min. The importance of post oxidation annealing has been reported in literature [9]. Post oxidation annealing has been found to reduce the amount of interface trap density (D_{it}) at the Al_2O_3/p- boron doped interface and recovery of Fermi level pinning [12].

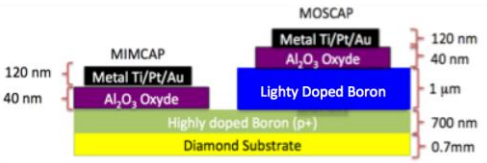

Fig. 1: Schematic of the MIMCAP and MOSCAP stacks

III. RESULTS AND DISCUSSIONS

Electrical characterizations have been performed in vacuum with the Modulab XM MTS system before and after the annealing process. C-V measurements have been performed at at 100 kHz. The leakage current measured before and after the annealing process was lower than 0.1 nA within the whole measurement range. No frequency dependence (at 10Hz - 1MHz) has been observed (graph not shown). C-V characteristic before annealing, presented in fig. 2a, exhibits a strong Fermi Level Pinning (FLP) effect. This explains the plateau observed on the CV at negative bias (< -2 V) and it originates from a high density of interface states in the diamond bad gap. Accumulation regime could not be obtained, in the range of measurements, because of the unexpected appearance of leakage current before filling all the interface states at the onset of the Fermi level pinning. The C-V characteristic after annealing presented in fig. 2a confirm that the annealing process leads to a substantial reduction of this effect and accumulation regime has been observed. C-V results presented in fig. 2a confirm that the annealing process leads to a substantial reduction of the Fermi level pinning. This can be attributed to the reduction of interface and oxide charge density due to rearrangement of the crystalline lattice at the diamond /Al_20_3 interface, similarly to what was observed on MOSCAP fabricated with UV-ozone treatment [9]. 95 % of the oxide capacitance was observed in accumulation after annealing. The flatband voltage (V_{FB}) was extracted from the intercept of the linear portion of Mott Schottky plot on the abscissa as shown in fig. 2b. A V_{FB} shift of -2.29 V was observed after annealing of the device. The V_{FB} shift induced by annealing from -3.53 V to -5.82 V (fig. 2b) seems to be of detrimental effect but leads to a more stable device as explained in the later section of this work. Annealing also induces a shift in the CV characteristics of the device. The shift in the CV characteristic has been monitored through a series of consecutive measurements and reported in the next section. The flatband voltage V_{FB} and the effective oxide charge N_{eff} have been extracted from these tests.

A. Monitoring flatband voltage shift by consecutive measurements

Several C-V measurements were performed at room temperature (RT). The main goal of the test is to ensure stable electrical parameters before performing the negative bias stress instability test (NBSI). At step time t_0, a gate bias was applied on the device sweeping from 5 V to -12 V, which corresponds to voltages in the deep depletion regime and accumulation regime respectively. A lower bias could lead to an increase of leakage current and a damage of the oxide layer. The sweep was applied 60 times with CV measurements performed for each voltage sweep. The device was then zero biased for a characteristic waiting time, t_{w1} = 1hr. The process was repeated for step t_1, t_2, and t_3 with t_{w2} = 5h, t_{w3} = 22 h. A schematic description of the measurement is shown in fig. 3.

The described measurement was carried out before and after the annealing process. The flatband voltage extracted for each CV measurement at different experimental step is shown in fig. 4. A significant shift in the flatband voltage is observed, but only between the first and second measurement of each experimental step. The obtained CV curve for first three measurements at step t_0 before annealing is shown in fig. 5a. The shift in the CV curve is noticed only after the first measurement indicating the maximum contribution of effective charges occurs between the first and second CV scans.

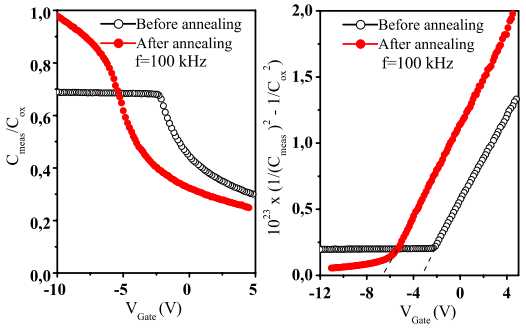

Fig. 2: (a) Normalized C(V_{Gate}) graph , right (b) Mott-Schottky plot before and after annealing, left

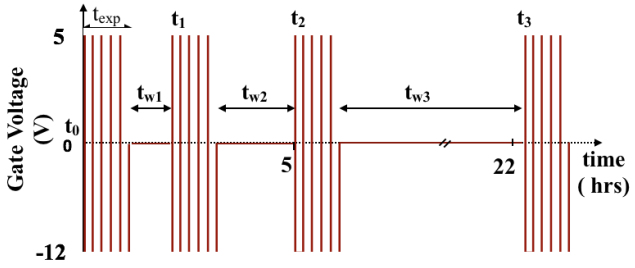

Fig. 3: Description of the consecutive CV measurements

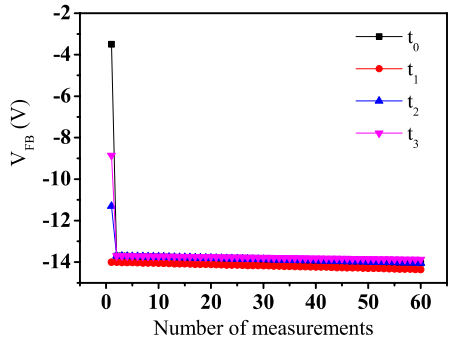

Fig. 4: Flatband voltage measured for 60 consecutive measurements in each experimental step measured before annealing

The correlation between the V_{FB} variation and the maximum amount of oxide charges N_{effmax} acting at the Al_2O_3/p- boron doped diamond interface during the consecutive measurement can be calculated using the following equation [13]:

$$N_{effmax} = \frac{-(V_{FBmin} - V_{fbth}) \times C_{OX}}{q \times A} \quad (1) \quad ;$$

where V_{fbth} = -2.6 eV is the theoretical flatband voltage, q is the electron charge, the effective MOSCAP metal gate area denoted by A, and V_{FBmin} the minimum negative flatband voltage extracted during the whole test. The flatband voltage obtained for the second measurement in each experimental step is considerably lower than V_{fbth} indicating the predominance of positive charges such as donor-like ion mobile charges or donor-like interface states that are excited during the measurement, as deduced from (1). It is difficult to clearly identify the defect or ion at the origin of this shift. But a recovery is observed without any bias (0V applied to the device), during waiting time t_w. The built in potential that exists at zero biais could explain the charge drift and consequent recovery.

B. Effects of annealing

From equation (1), the calculated oxide charges responsible for shift of the CV characteristic is 5.6 x 10^{12} cm^{-2} before annealing and 3.9 x 10^{11} cm^{-2} after annealing. The obtained values show that there could be a reduction in the near interface defects due to the post oxidation annealing. To investigate further the effect of annealing, the flatband voltage, V_{FB} obtained for the first (of 60 consecutive measurements) in each experimental step (i.e. t_0, t_1, t_2, t_3) before and after annealing is plotted versus time fig. 5(b). Before annealing, more than -10 V difference is observed between the V_{fb} (t_0) and V_{fb} (t_1). For experimental step t_3 after t_{w3} = 22 hrs, the V_{fb} does not recover back to the initial value at t_0. However, after annealing, the difference between V_{fb} (t_0) and V_{fb} (t_1) is reduced to 1.5V at t_3, V_{fb} is closer to the theoretical value. From these results, we suggest that annealing could have changed the energy position of the interface states within the band gap, and neutralized the effect of some traps and interface states that were responsible of the flatband voltage drift. The post oxidation annealing shows positive effects and decreases the amount of effective charge at the Al_2O_3/diamond interface.

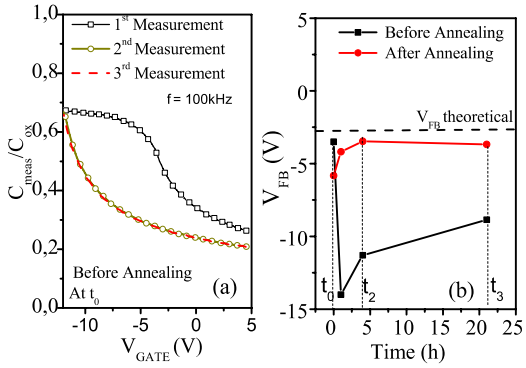

Fig. 5: (a) CV graph of the first, second and third measurement at step t_0 performed before annealing and (b) V_{FB} variation as a function of time t_n extracted before and after annealing

C. Flatband Variation by Negative Bias Instability Technique (NBSI)

This method has been reported in the literature for silicon carbide MOSFET [13] and applied to a test device after annealing process. The negative bias stress instability technique has been applied on the annealed diamond p-type MOSCAP in order to evaluate the oxide electrical stability. The experiment is described (fig. 6) in two steps.

a) Application of voltage bias from +5 V to -10 V in a CV measurement condition.
b) A constant negative bias stress of -10 V was applied on the device for a defined bias stress time t_b, in order to accumulate holes at the interface.

The process was done for t_{b1} = 10 s, t_{b2} =100 s, t_{b3} = 500 s, t_{b4} = 1000 s, t_{b5} = 1200 s, t_{b6} =1500 s. The CV graph and the flatband voltage extracted after each bias stress time is shown in fig. 7. The simulated curve depicted in fig. 7a., corresponding

to an ideal MOSCAP, is calculated from the Poisson equation assuming no oxide or interface states.

A decrease in the flatband voltage is clearly observed with increasing bias stress time signifying an increase in the effective oxide charges as shown in fig. 7b. However after 1500s, this drift variation is less than 1V, resulting in an increase of effective oxide charge of less than 5 x 10^{11} cm^{-2}.

That is the first time that such NBSI experiemnts are performed on diamond, and therefore the first time such shift is observed. The mechanism is not clear. A two way tunneling model [21] could explain the flatband voltage shift under the bias stress time. The magnitude of the stress time determines which oxide traps may change charge state during the stress and the magnitude of shift observed. The longer the stress time the deeper into the oxide traps that can be excited. Hence, the progressive increase in observed shift with bias stressing time. Using (1) and the minimum flatband voltage, the total amount of effective, N_{efftot}= 9.8 x 10^{11} cm^{-2}. This value is comparable to those observed in 4H-SiC MOSCAP [13], [14] and confirms the good oxide quality of Al_2O_3 layer aided by annealing process. We could expect an increase in the flatband shift with longer bias stress time till saturation is attained. A possible improvement in the device processing parameters can improve the stability of this studied device.

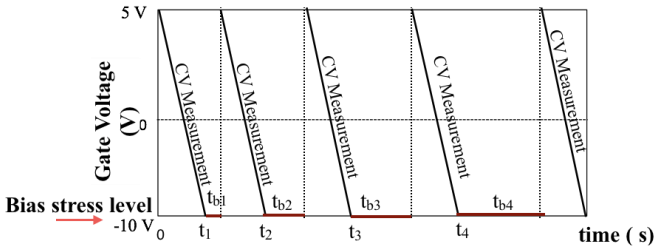

Fig. 6: Experimental description of the negative stress bias instability test.

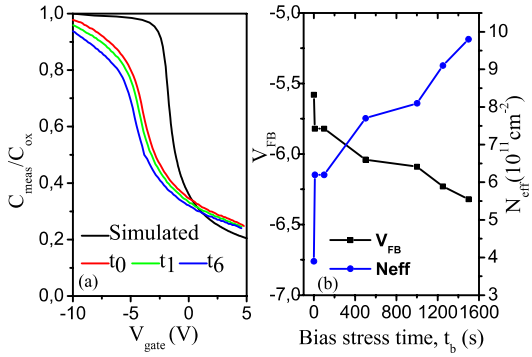

Fig. 7: (a) Normalized C(V) graph for the different stress type and (b) flatband voltage (square, left) and oxide charge (circle, right) variations with stress time. All measurements were done on annealed sample.

IV. Conclusion

A reliability study for diamond MOS capacitors has been proposed for the first time in this work. We have shown that, in order to perform a correct analysis of the flatband voltage stability and to extract the effective oxide charge at the Al_2O_3/boron doped diamond interface, an initialization C (V) test is required. This test was necessary to stabilize the device prior to performing the negative bias stress test. In addition, the reduction of the Fermi level pinning together with the increased stability of the flatband voltage have confirmed the benefits of the high temperature post-oxidation annealing process on Al_2O_3/boron doped diamond interfaces.

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